Title: Relaxed SiGe Platform for High Speed CMOS
Electronics and High Speed Analog Circuits
Inventor: Fitzgerald
Serial No.: Not Yet Assigned
Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
Formal Drawing Sheet 1 of 17

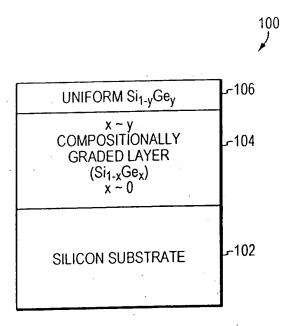


FIG. 1

Title: Relaxed SiGe Platform for High Speed CMOS
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Inventor: Fitzgerald
Serial No.: Not Yet Assigned
Atty Docket No.: ASC-049C!
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
Formal Drawing Sheet 2 of 17

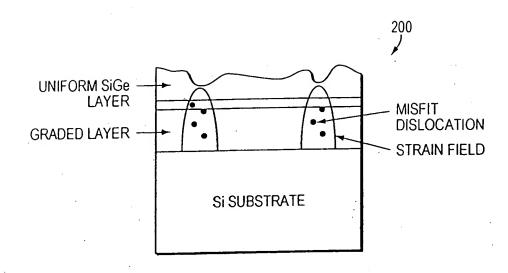


FIG. 2

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 3 of 17

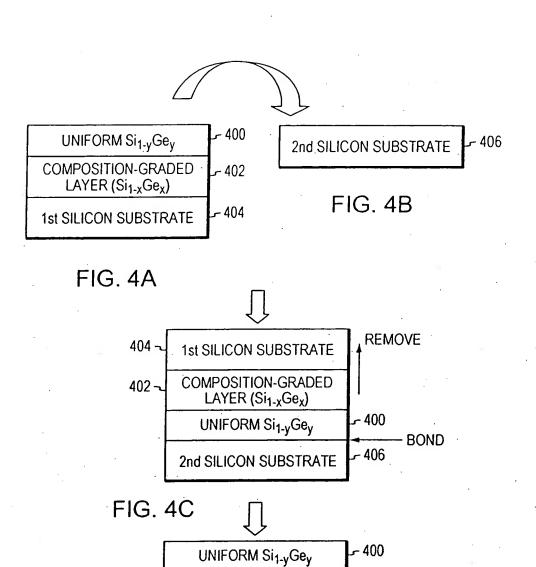
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TYPE OF SURFACE	AVERAGE ROUGHNESS (nm)
AS-GROWN GRADED COMPOSITION RELAXED SiGe PLANARIZED SIGE REGROWTH SIGE, LATTICE-MATCHED REGROWTH SIGE, LIGHT MISMATCH, THICKNESS = 1.5 µm	7.9 0.57 ~0.6 0.77

FIG. 3

Title: Relaxed SiGe Platform for High Speed CMOS
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2nd SILICON SUBSTRATE

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FIG. 4D

Title: Relaxed SiGe Platform for High Speed CMOS
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Inventor: Fitzgerald
Serial No.: Not Yet Assigned
Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
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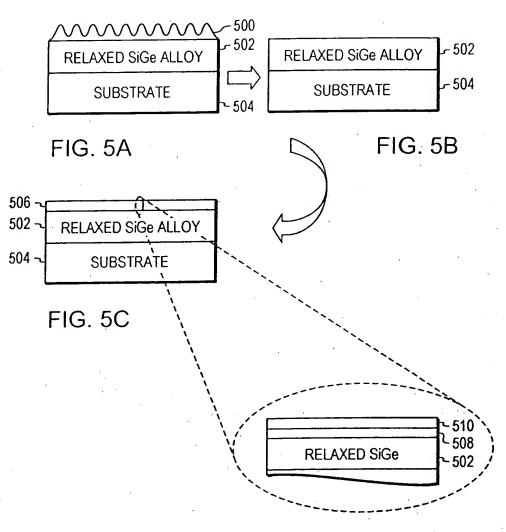
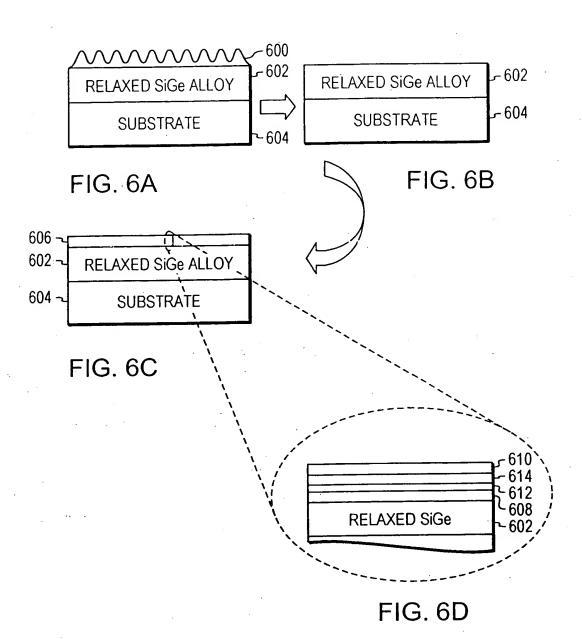


FIG. 5D ~

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald
Serial No.: Not Yet Assigned
Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
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Title: Relaxed SiGe Platform for High Speed CMOS
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Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
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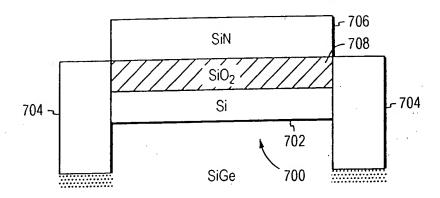


FIG. 7A

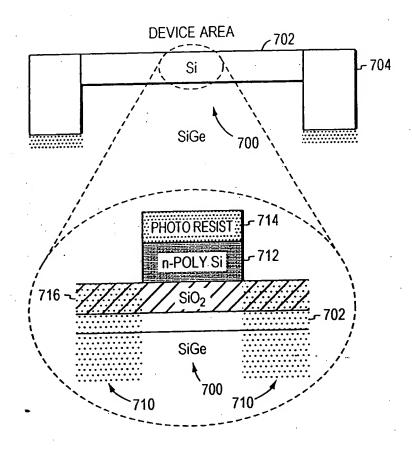


FIG. 7B

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald
Serial No.: Not Yet Assigned
Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
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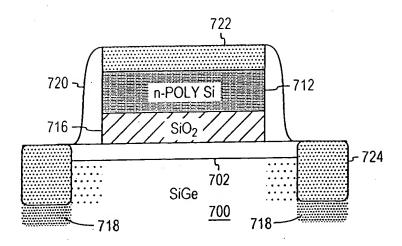


FIG. 7C

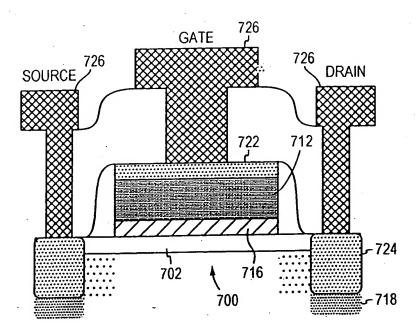


FIG. 7D

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 9 of 17

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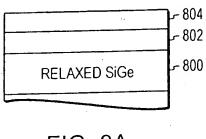


FIG. 8A

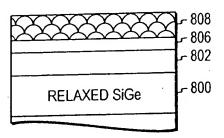


FIG. 8B

Title: Relaxed SiGe Platform for High Speed CMOS
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Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
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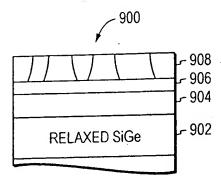


FIG. 9A

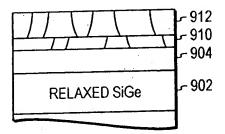


FIG. 9B

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Serial No.: Not Yet Assigned
Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
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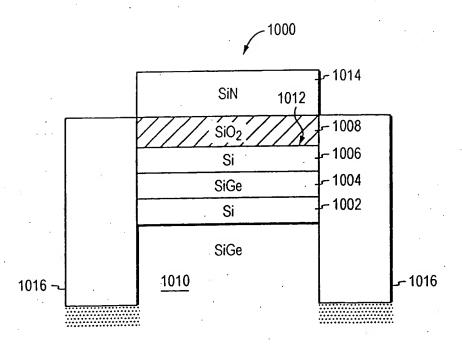


FIG. 10

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald

Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov

Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 12 of 17

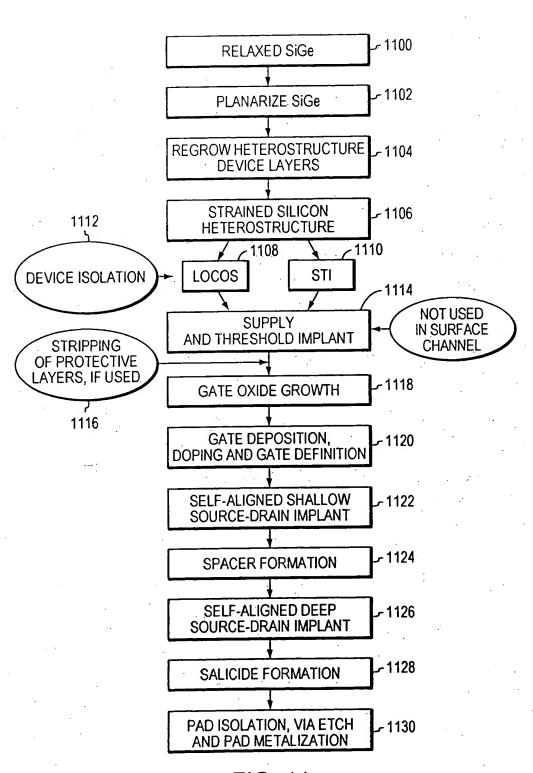


FIG. 11

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1

Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 13 of 17

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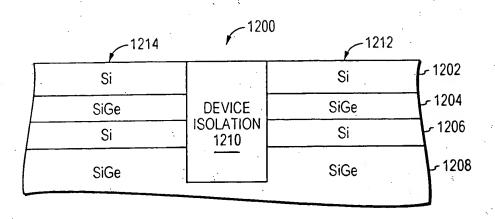


FIG. 12A

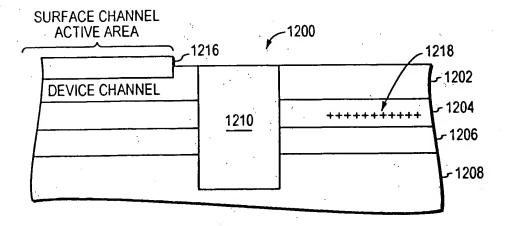


FIG. 12B

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald

Serial No.: Not Yet Assigned

Serial No.: Not Yet Assigned
Atty Docket No.: ASC-049C1
Atty: Mark L. Beloborodov
Express Mail Mailing Label No.: EL 988705761 US
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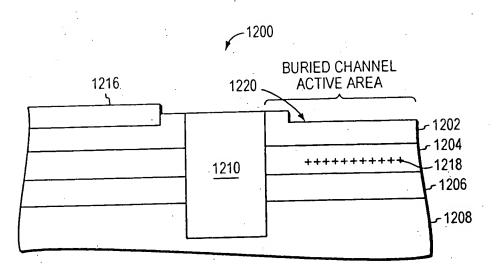


FIG. 12C

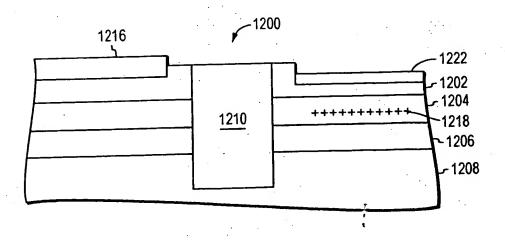


FIG. 12D

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov

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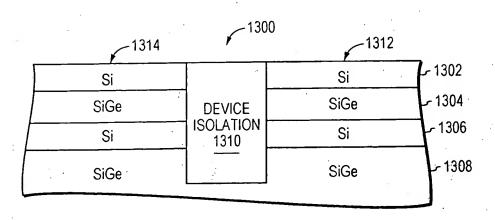
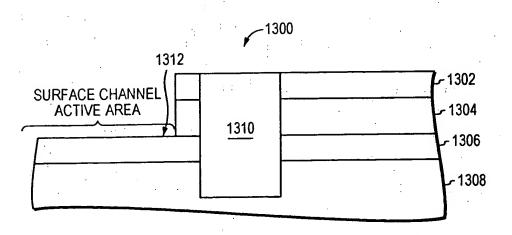


FIG. 13A



FIG; 13B

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 16 of 17

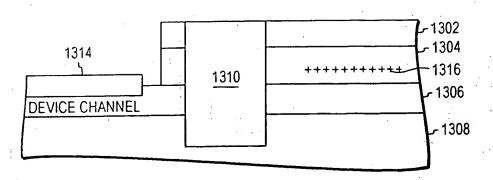


FIG. 13C

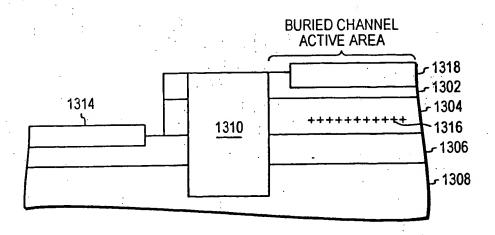


FIG. 13D

Title: Relaxed SiGe Platform for High Speed CMOS Electronics and High Speed Analog Circuits Inventor: Fitzgerald Serial No.: Not Yet Assigned Atty Docket No.: ASC-049C1 Atty: Mark L. Beloborodov Express Mail Mailing Label No.: EL 988705761 US Formal Drawing Sheet 17 of 17

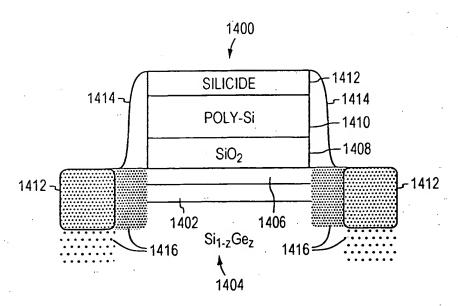


FIG. 14A

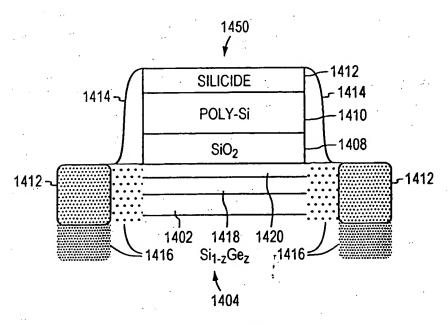


FIG. 14B